TBM Selection Criteria

Cristian Gingu
- for Fermilab FPIX group -

Parameters' Cut Values

1. For each test, set the cuts you want to apply. Set also the gain classes (like G300,G500…).

2048			TIME		GAIN			LIN		RegEA				RegEC				RegEE			
120	RE	FE	RE	FE	BL	UB	L0	Slop	Inter	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

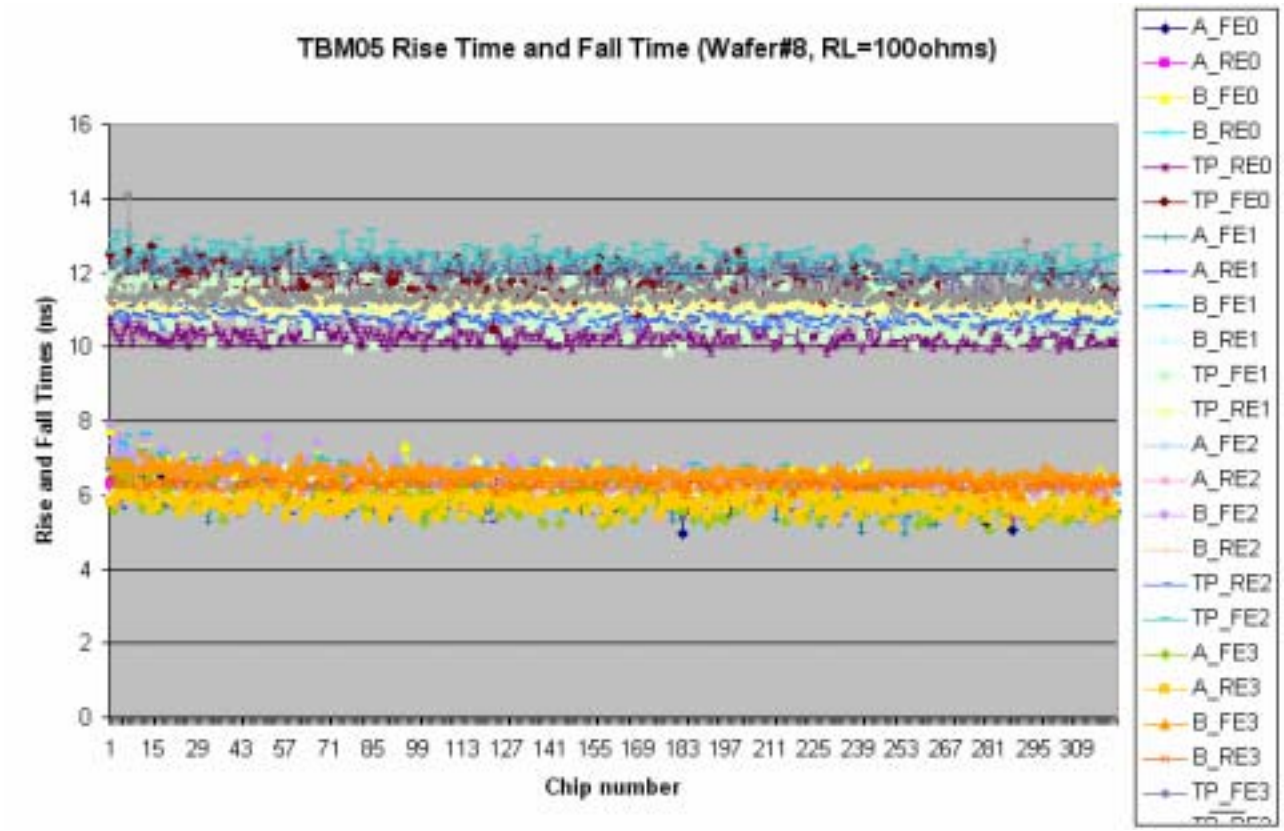
2. Start the code. Load test data files (two files per wafer, analog and digital). The chips passing the above selection are reported.

TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	6	YIELD (%)	MAR GINAL
321	80	528	0	45	0	73	8	1	G500	182	60.80	127
				0_0_0	0_0	0_0_1	0_0_0	0_1_0	G700	130		
									G900	3		

UB and TP Rise and Fall Times

2048	TIME				GAIN			LIN		RegEA				RegEC				RegEE			
120	RE	FE	RE	FE	BL	UB	L0	Slop	Inter	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

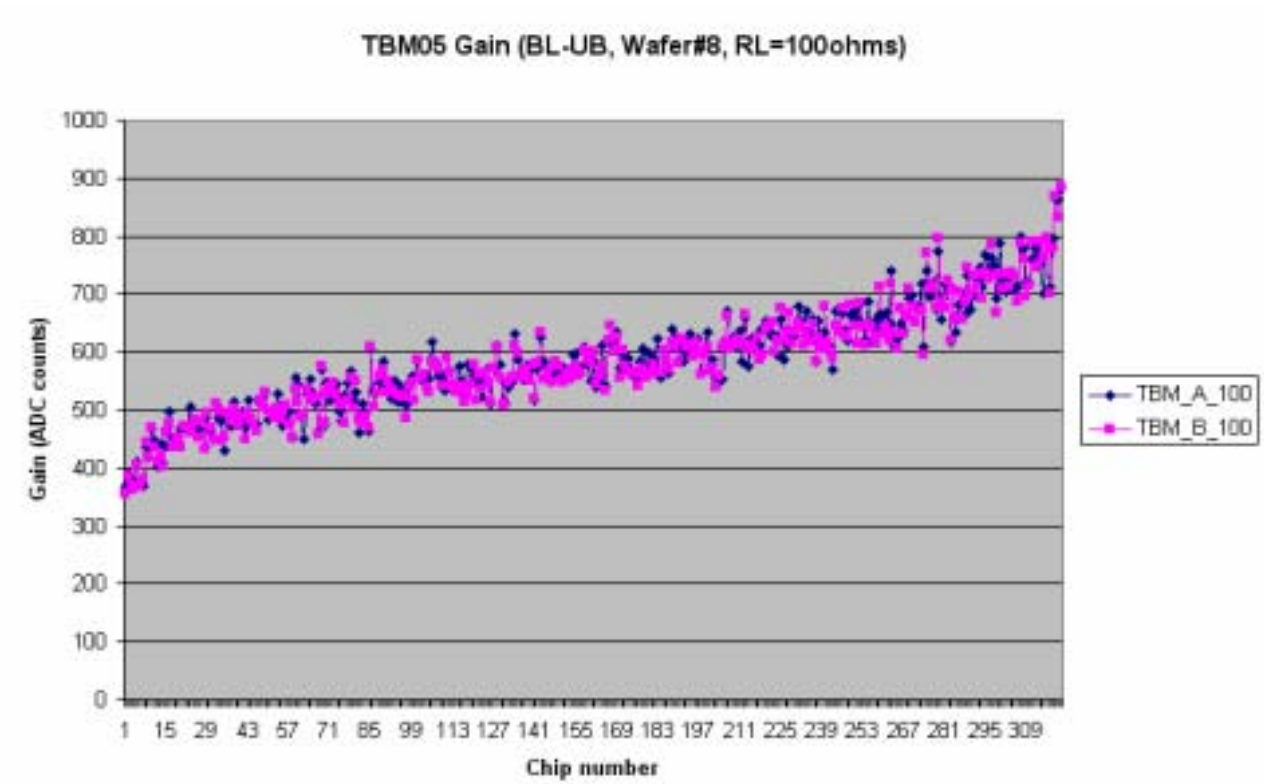
TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	6	YIELD (%)	MARGINAL
321	80	528	0	45	0	73	8	1	G500	182	60.80	127
				0_0_0	0_0	0_0_1	0_0_0	0_1_0	G700	130		
									G900	3		



Gain Cuts

2048	TIME				GAIN			LIN		RegEA				RegEC				RegEE			
120	RE	FE	RE	FE	BL	UB	L0	Slop	Inter	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

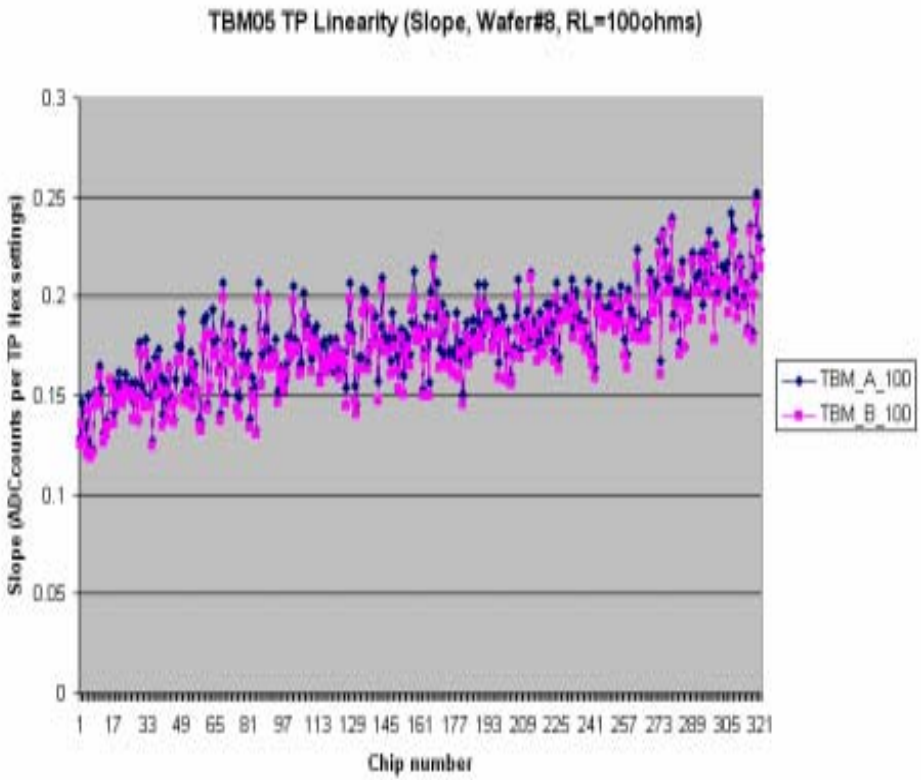
TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	6	YIELD (%)	MARGINAL
321	80	528	0	45	0	73	8	1	G500	182	60.80	127
				0_0_0	0_0	0_0_1	0_0_0	0_1_0	G700	130		
									G900	3		

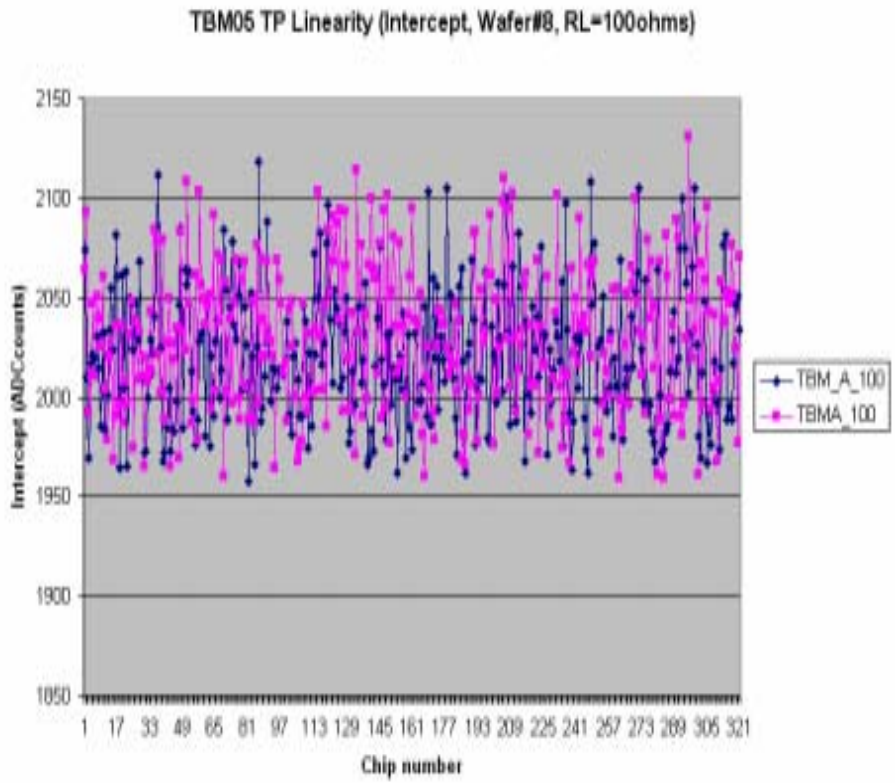


TP Linearity Cuts

2048	TIME				GAIN			LIN		RegEA				RegEC				RegEE			
120	RE	FE	RE	FE	BL	UB	L0	Slop	Inter	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	6	YIELD (%)	MARGINAL
321	80	528	0	45	0	73	8	1	G500	182	60.80	127
				0_0_0	0_0	0_0_1	0_0_0	0_1_0	G700	130		
									G900	3		

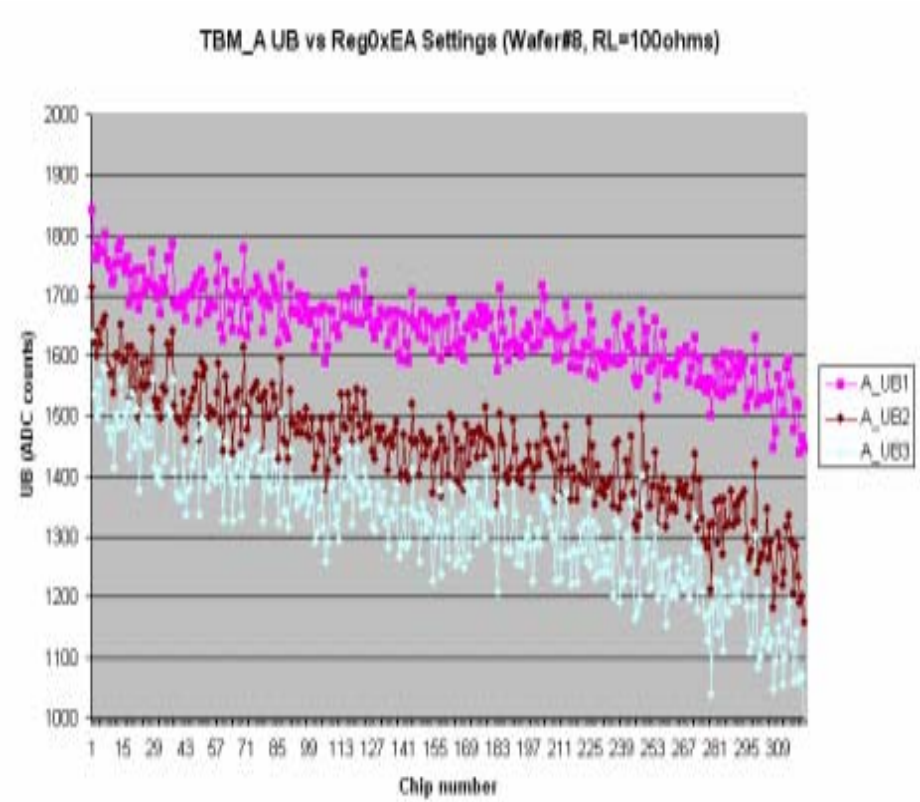


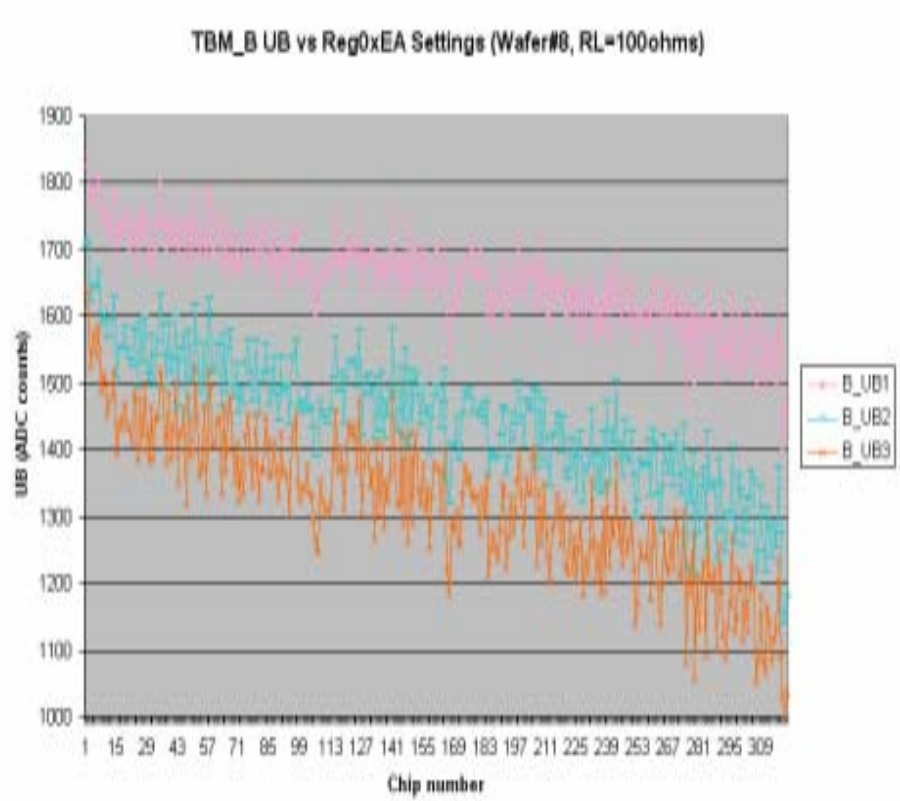


TP Register 0xEA Cuts

2048	TIME				GAIN			LIN		RegEA				RegEC				RegEE			
120	RE	FE	RE	FE	BL	UB	L0	Slop	Inte	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	6	YIELD (%)	MARGINAL
321	80	528	0	45	0	73	8	1	G500	182	60.80	127
				0_0_0	0_0	0_0_1	0_0_0	0_1_0	G700	130		
									G900	3		

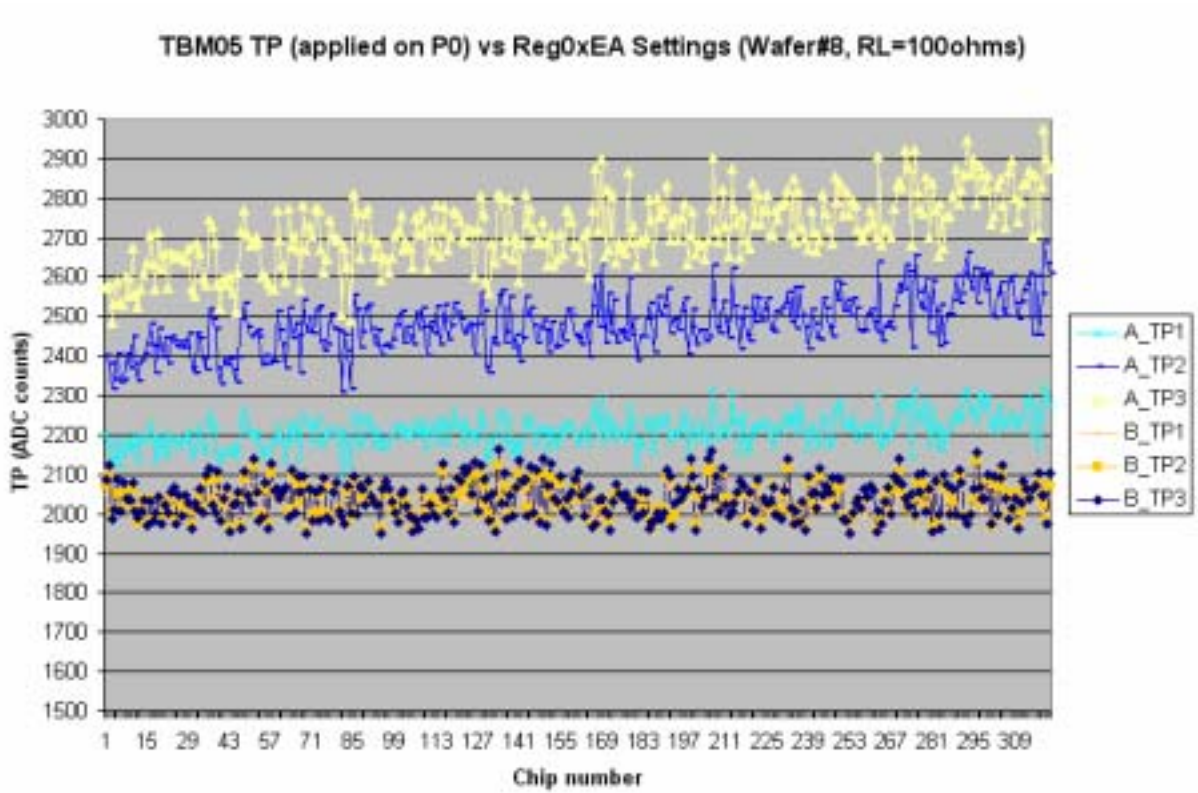




TP Register 0xEA Cuts

2048	TIME				GAIN			LIN		RegEA				RegEC				RegEE			
120	RE	FE	RE	FE	BL	UB	L0	Slop	Inte	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

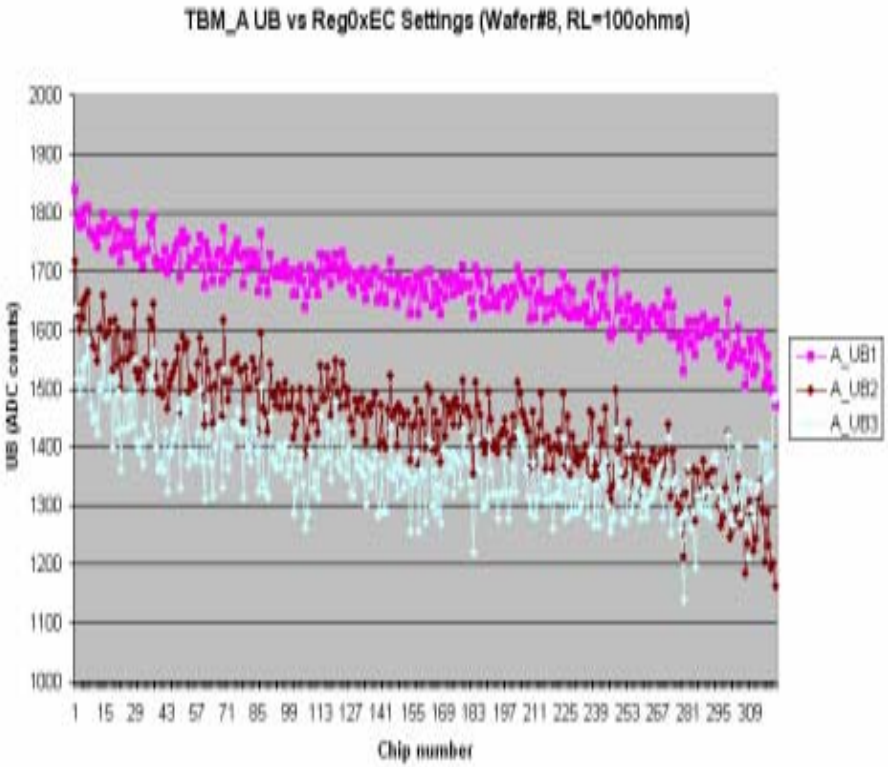
TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	6	YIELD (%)	MARGINAL
321	80	528	0	45	0	73	8	1	G500	182	60.80	127
				0_0_0	0_0	0_0_1	0_0_0	0_1_0	G700	130		
									G900	3		

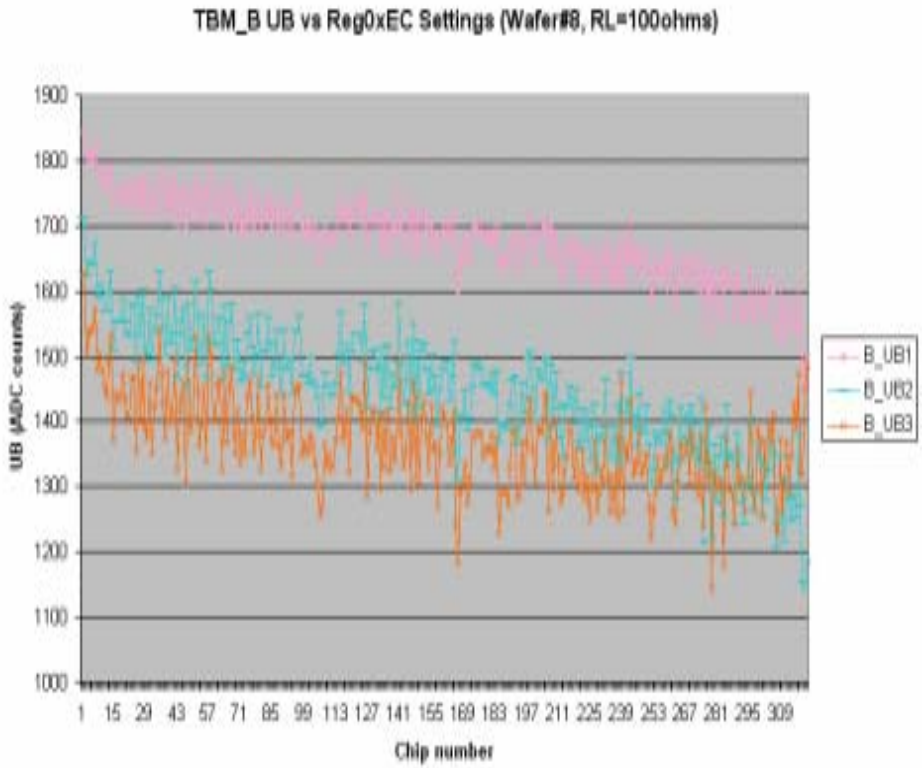


TP Register 0xEC Cuts

2048	TIME				GAIN			LIN		RegEA				RegEC				RegEE			
120	RE	FE	RE	FE	BL	UB	L0	Slop	Inter	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	6	YIELD (%)	MARGINAL
321	80	528	0	45	0	73	8	1	G500	182	60.80	127
				0_0_0	0_0	0_0_1	0_0_0	0_1_0	G700	130		
									G900	3		

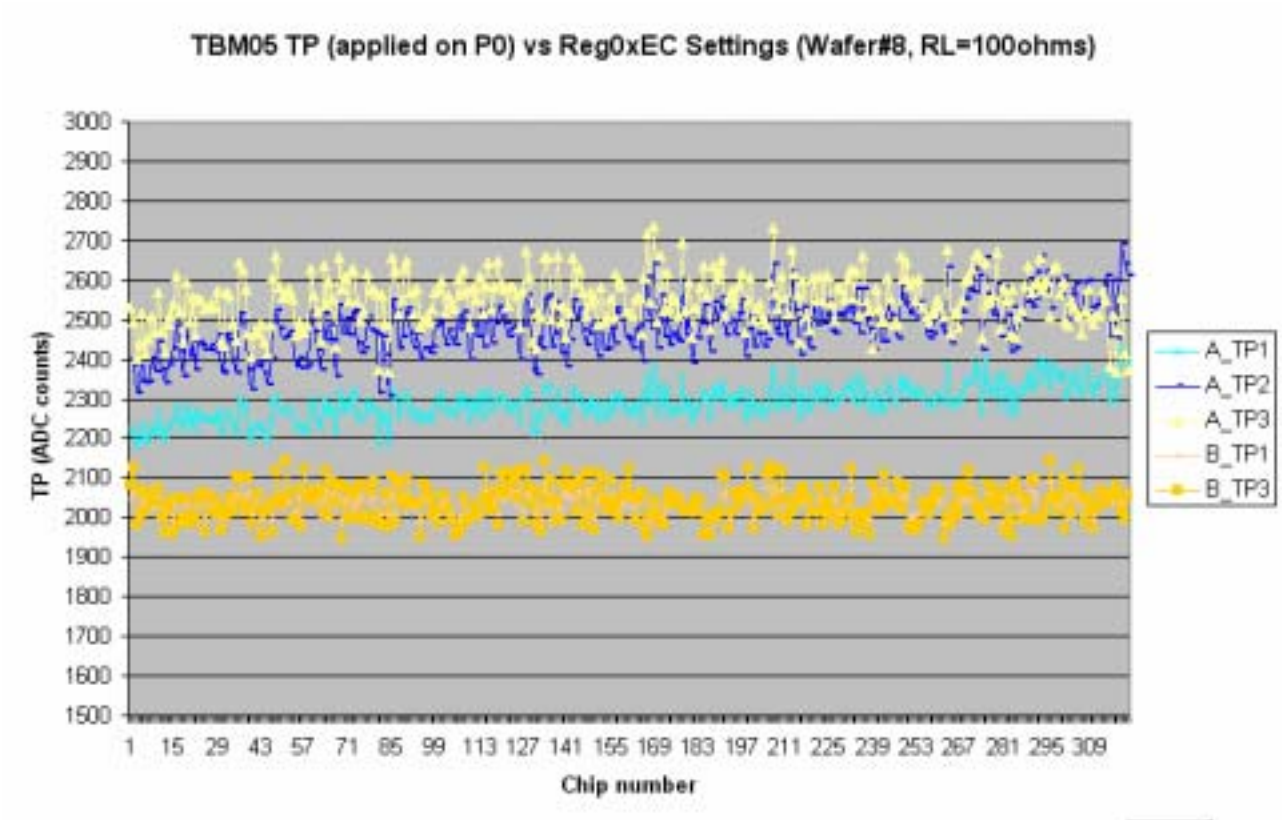




TP Register 0xEC Cuts

2048	TIME				GAIN			LIN		RegEA				RegEC				RegEE			
120	RE	FE	RE	FE	BL	UB	L0	Slop	Inter	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

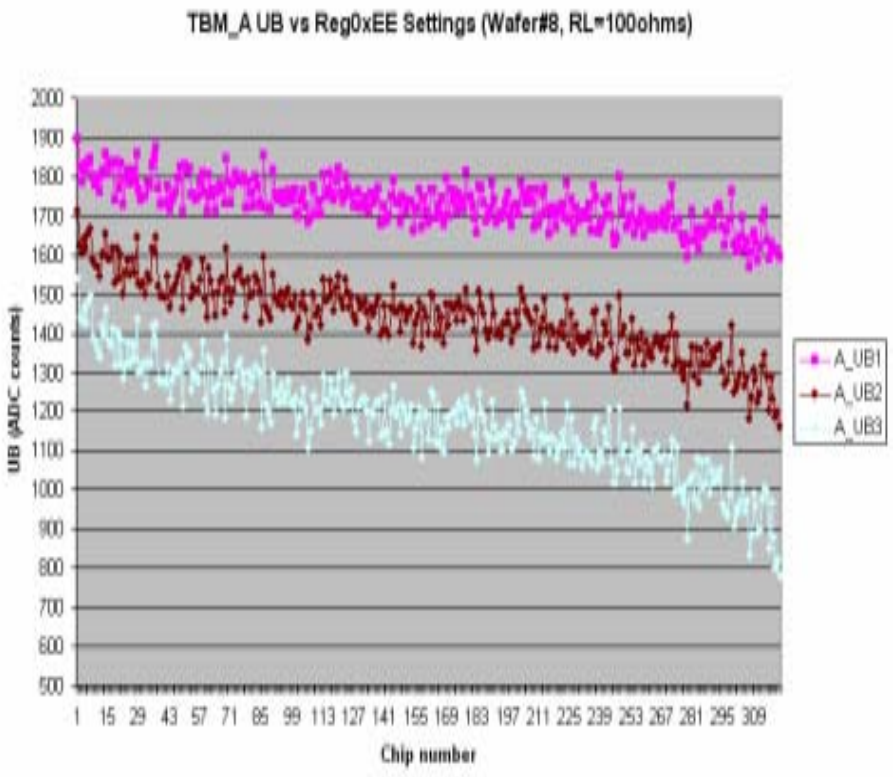
TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	6	YIELD (%)	MARGINAL
321	80	528	0	45	0	73	8	1	G500	182	60.80	127
				0_0_0	0_0	0_0_1	0_0_0	0_1_0	G700	130		
									G900	3		

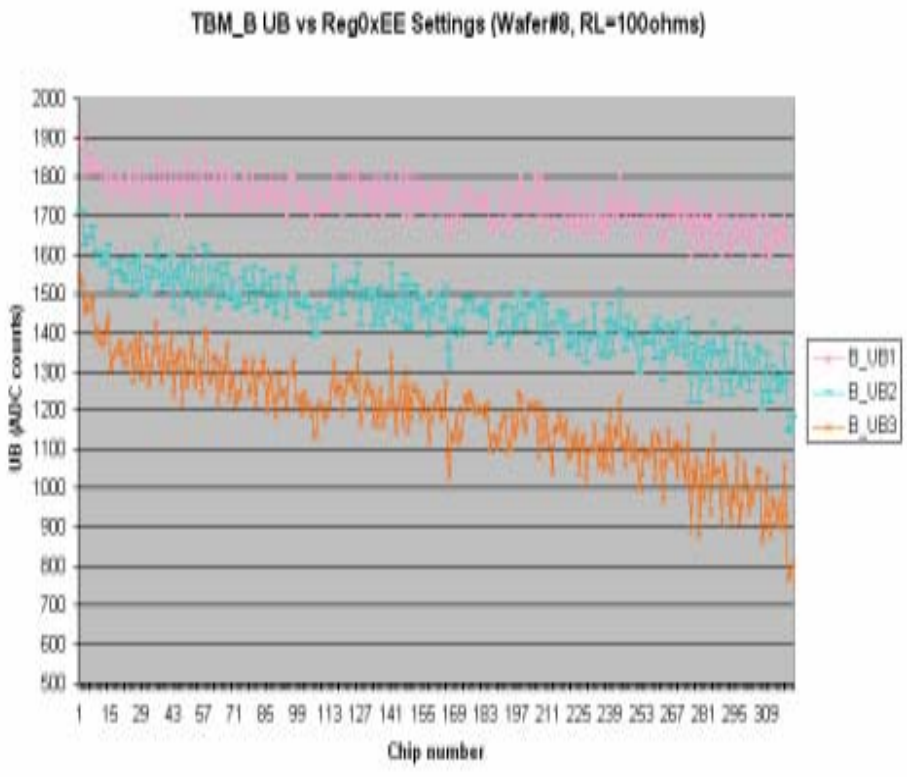


TP Register 0xEE Cuts

2048	TIME				GAIN			LIN		RegEA				RegEC				RegEE			
120	RE	FE	RE	FE	BL	UB	L0	Slop	Inter	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	6	YIELD (%)	MARGINAL
321	80	528	0	45	0	73	8	1	G500	182	60.80	127
				0_0_0	0_0	0_0_1	0_0_0	0_1_0	G700	130		
									G900	3		

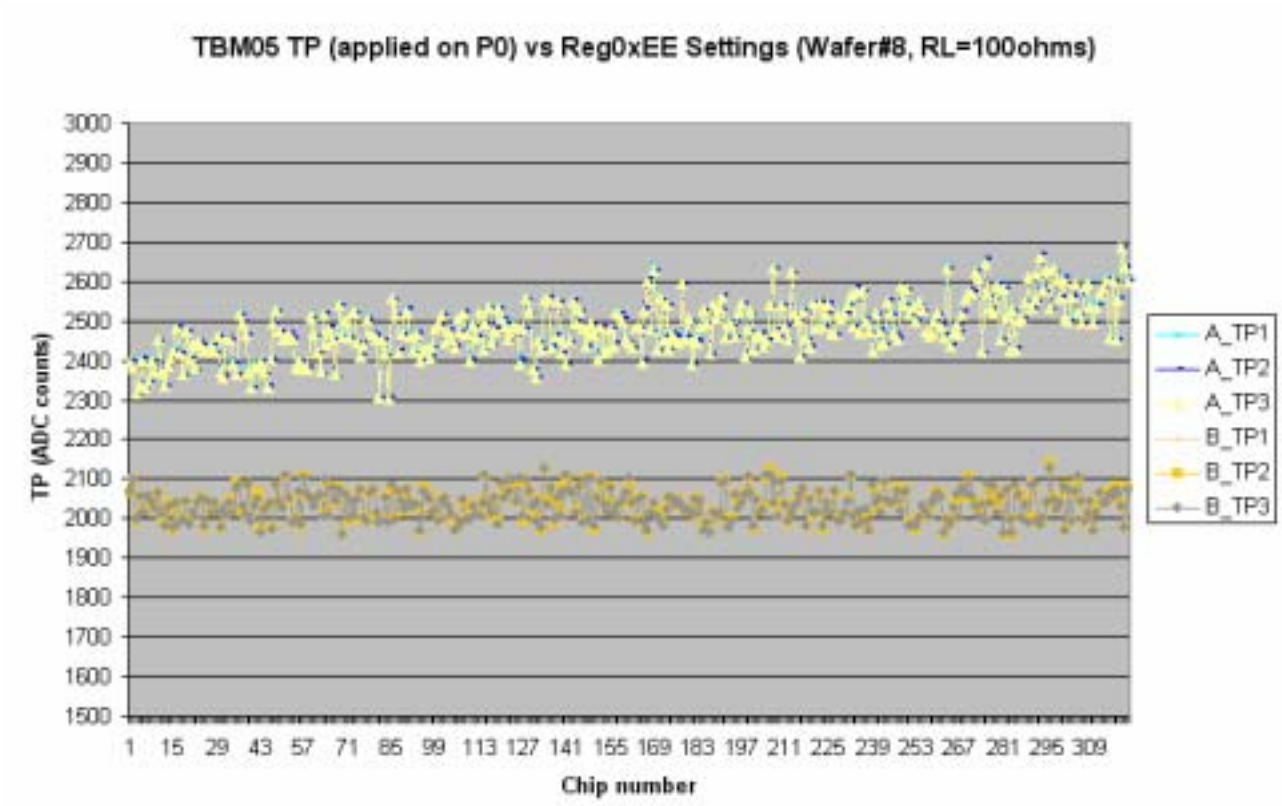




TP Register 0xEE Cuts

2048	TIME				GAIN			LIN		RegEA				RegEC				RegEE			
120	RE	FE	RE	FE	BL	UB	L0	Slop	Inter	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

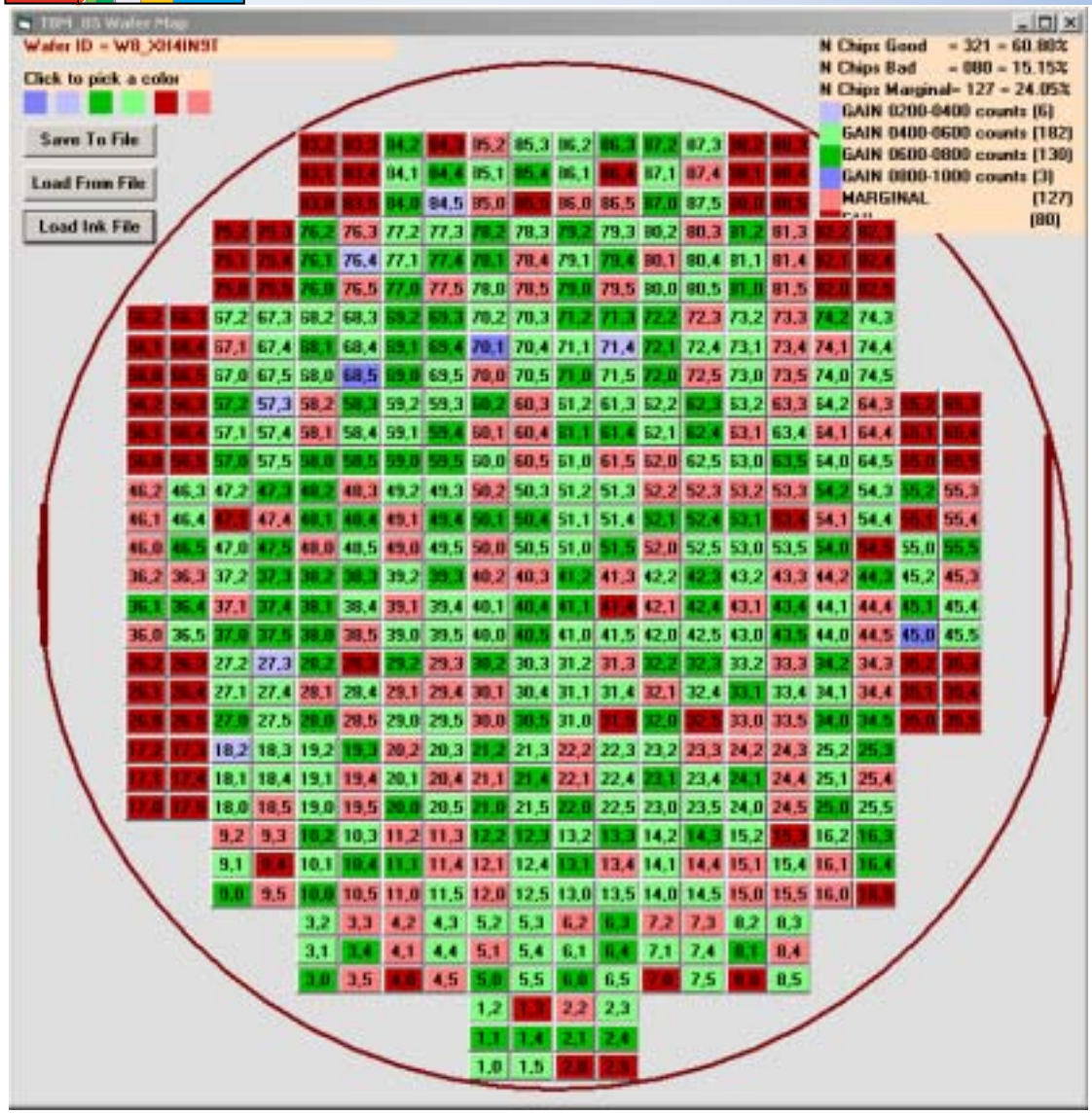
TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	6	YIELD (%)	MARGINAL
321	80	528	0	45	0	73	8	1	G500	182	60.80	127
				0_0_0	0_0	0_0_1	0_0_0	0_1_0	G700	130		
									G900	3		

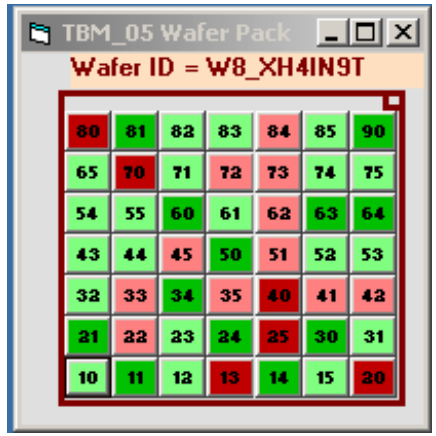


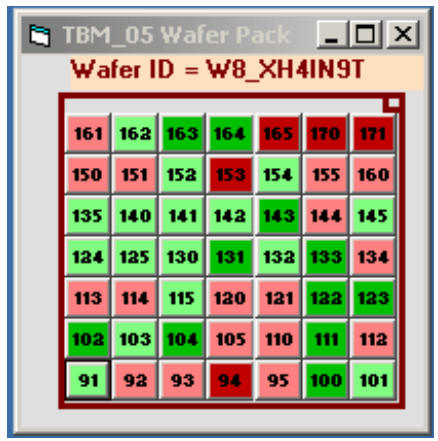
Other Analog Cuts

01 000500 001500	'Idig	= 5 to 15 mA
02 000500 002500	'Iana	= 10 to 25 mA for TBM05, 5 to 15 mA for TBM04
03 001800 002400	'Vcapva	= 1.8 to 2.4 V
04 001800 002400	'Vcapvd	= 1.8 to 2.4 V
05 000700 001300	'Vcaplvdslow	= 0.7 to 1.3 V
06 000900 001500	'Vcaplvdshigh	= 0.9 to 1.5 V

Wafer Map (Dicing Company)







Base Line Cuts Comparison

2048 120	TIME				GAIN			LIN		RegEA				RegEC				RegEE			
	RE	FE	RE	FE	BL	UB	L0	Slop	Inter	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	6	YIELD (%)	MARGINAL
321	80	528	0	45	0	73	8	1	G500	182		
									G700	130	60.80	127
				0_0_0	0_0	0_0_1	0_0_0	0_1_0	G900	3		

2048 200	TIME				GAIN			LIN		RegEA				RegEC				RegEE			
	RE	FE	RE	FE	BL	UB	L0	Slop	Inter	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
min	4	4	9	9	1848		1848	0.1	1848	1848	100	1848	100	1848	100	1848	100	1848	100	1848	1800
max	8	8	15	15	2248		2248	0.3	2248	2248	50	2248	50	2248		2248		2248	50	2248	2700

TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	7	YIELD (%)	MARGINAL
440	80	528	0	0	0	7	0	1	G500	242		
									G700	185	83.33	8
				0_0_0	0_0	0_0_0	0_0_0	0_1_0	G900	6		

Base Line (Offset) Classes

Offset Class	2048	TIME				GAIN			LIN		RegEA				RegEC				RegEE			
	120	RE	FE	RE	FE	BL	UB	L0	Slop	Inter	BL	UB	L0	TP	BL	UB	L0	TP	BL	UB	L0	TP
40	min	4	4	9	9	1928		1928	0.1	1928	1928	100	1928	100	1928	100	1928	100	1928	100	1928	1800
	max	8	8	15	15	2168		2168	0.3	2168	2168	50	2168	50	2168		2168		2168	50	2168	2700

TOTAL PASS	DIGITAL FAIL=1	TOTAL CHIPS	TIME FAIL=2	GAIN_BL FAIL=3	LIN FAIL=4	RegEA FAIL=5	RegEC FAIL=6	RegEE FAIL=7	G300	6	YIELD (%)	MARGINAL
321	80	528	0	45	0	73	8	1	G500	182	60.80	127
				0_0_0	0_0	0_0_1	0_0_0	0_1_0	G700	130		
									G900	3		

As described in slide 1, chips are assigned different classes based on Gain measurements (like G300 for Gain within 200 and 400 ADC counts). It was suggested to do a similar classification based on offset values.

A chip is assigned an Offset Class depending on Base Line measured values. This is done independently for TBM sections A and B.

If BL class width is defined to be 40 ADC counts (as above), then:

- Class 0 <=> BL between (2028,2068)
- Class -1 <=> BL between (1988,2028), Class -2 <=> BL between (1948,1988)…
- Class 1 <=> BL between (2068, 2108), Class 2 <=> BL between (2108,2148)…

For example, a chip with TBM A Base Line of 2000 ADC counts and TBM B Base Line of 2150 ADC counts will be assigned the class BL-1+3 i.e. the Base Line class is -1 for TBM A and +3 for TBM B.

Wafer Report Files

After running the code with some selection criteria, the following three files are generated for each wafer:

1. A special file used for automatic wafer ink dot placement.
2. A special file used for wafer map generation (see slide 13).
3. A text file that reports each chip's Gain and Base Line classes. This might be used for TBM chip selection while assembling the modules. It contains (see example below) the testing date, reticule and chip number, a PASS/FAIL string with the test selection criteria that failed, the Gain Class and finally the Base Line Class.

2/28/2006	40	4	PASS	0	G500	BL-2+3
2/28/2006	8	0	PASS	0	G700	BL-1-2
2/28/2006	52	3	PASS	0	G500	BL-2+1
.....						
2/28/2006	54	0	FAIL	1	F1	
.....						
2/28/2006	37	3	FAIL	2	G300	BL-3-1
2/28/2006	14	1	FAIL	3	G500	BL-4-1
2/28/2006	14	5	FAIL	6	G500	BL-3-2
.....						
3/1/2006	73	4	FAIL	6	G700	BL-3+2
2/28/2006	39	2	FAIL	32	Ghigh	BL-2-1

Base Line Classes Approach

The TBM Base Line is measured many times while the chip is tested. To assign a Base Line Class, we can use all the available measurements or just some of them. There are seven tests providing base line data: one Gain test (with Test Pulse applied at Port P0), three analog registers (0xEA, 0xEC and 0xEE) scan tests with Test Pulse applied to TBM A Port 0 and another three when the Test Pulse is applied to TBM B Port 2.

We observed that the Base Line value is changing while the analog register settings are changed. This is not a desired effect. To understand how much this affects the Base Line Class assignment we do compare in following four scenarios for class assignment procedure:

CASE 1. Consider BL data from all seven test and take the worst case value.

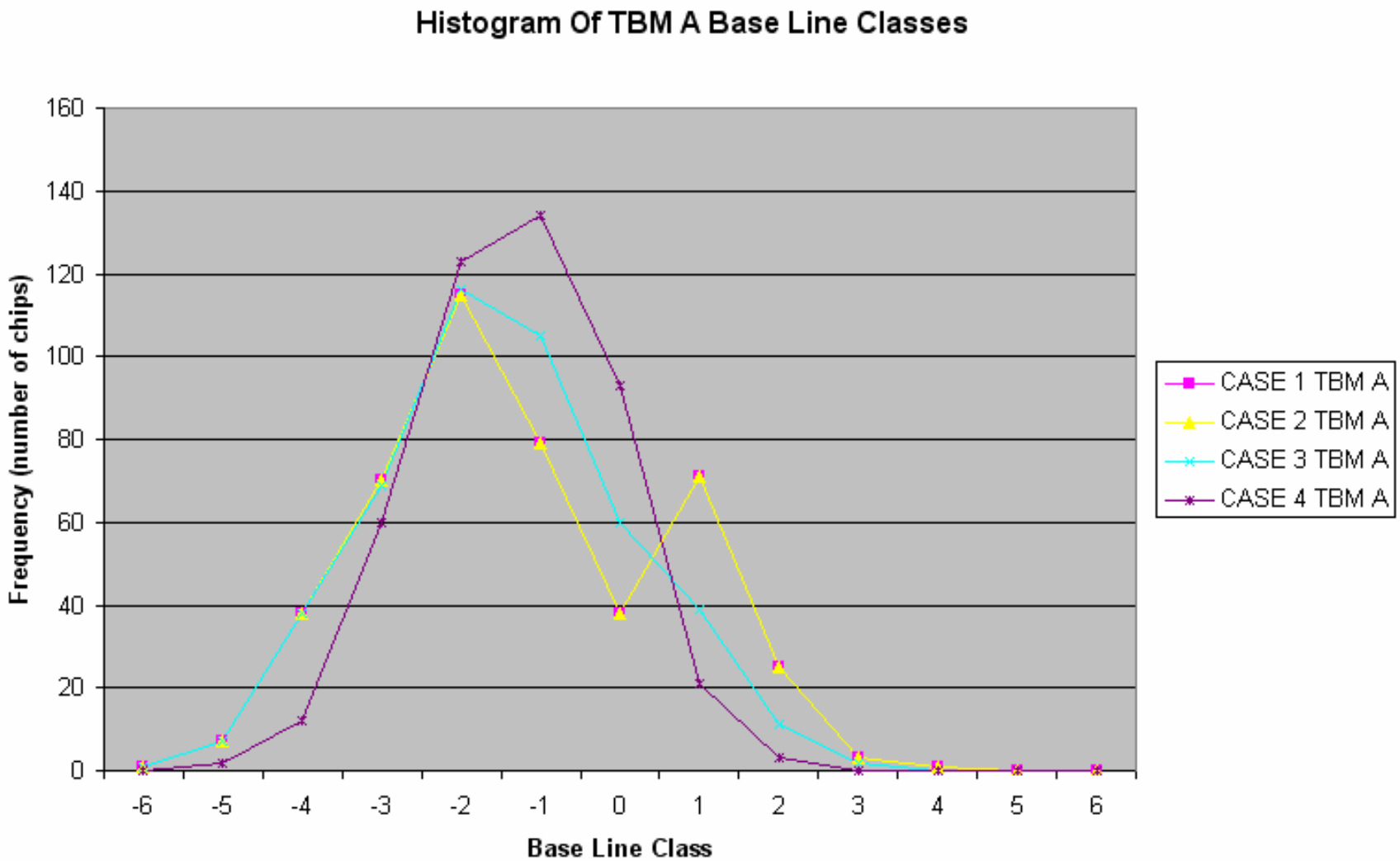
CASE 2. Exclude data from Gain test and consider all register scan tests, regardless of what TBM port the Test Pulse is applied to.

CASE 3. Consider all six register scan tests but exclude, for each TBM section, the measurements when Test Pulse is applied to that section.

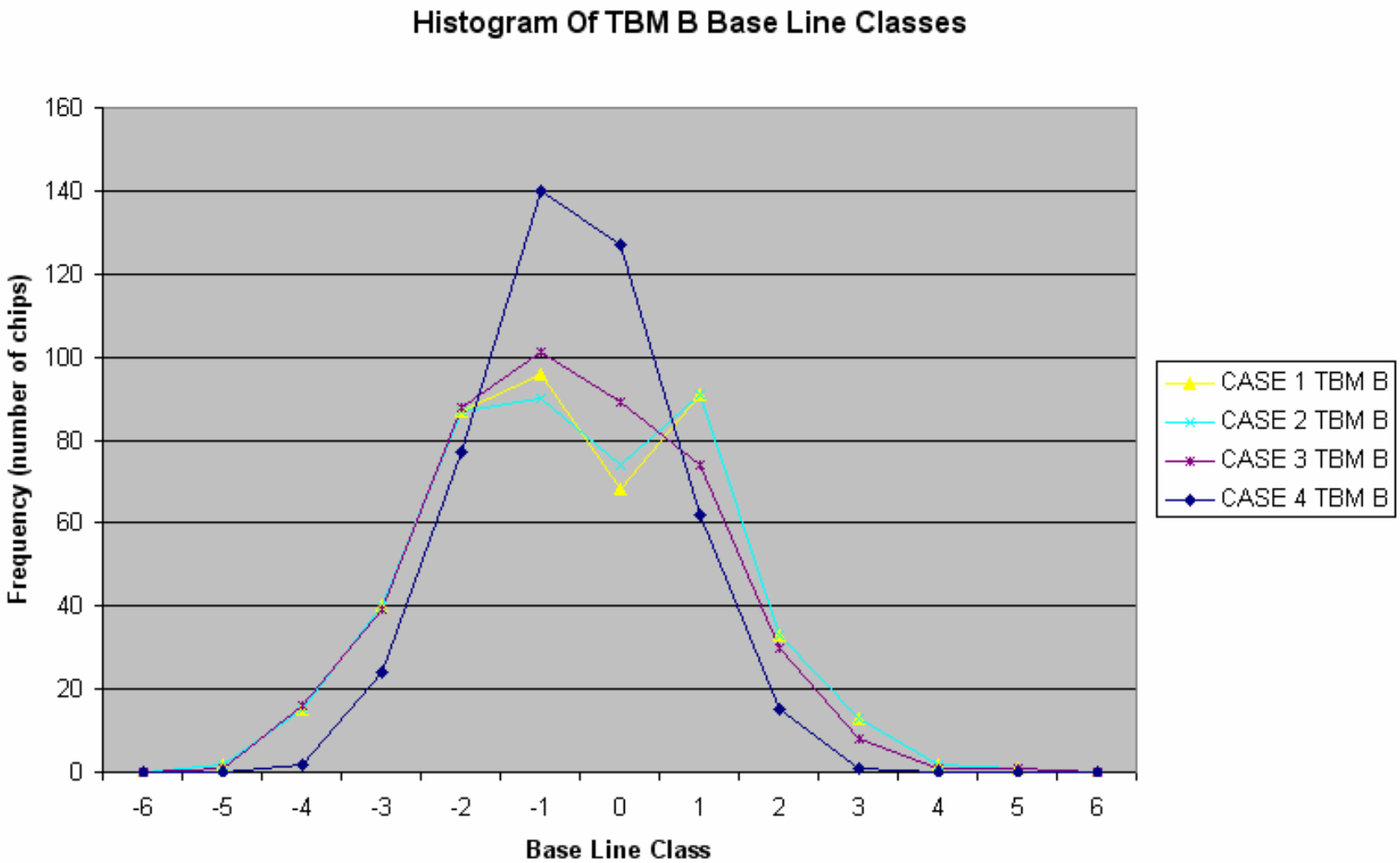
CASE 4. Same as last scenario and on top of that consider only the BL values measured for default register setting (0x80).

The Base Line histogram obtained from measured data on one wafer are presented in next slides. No significant change can be observed. For conservative reasons, we propose to stick with the most general scenario (CASE 1).

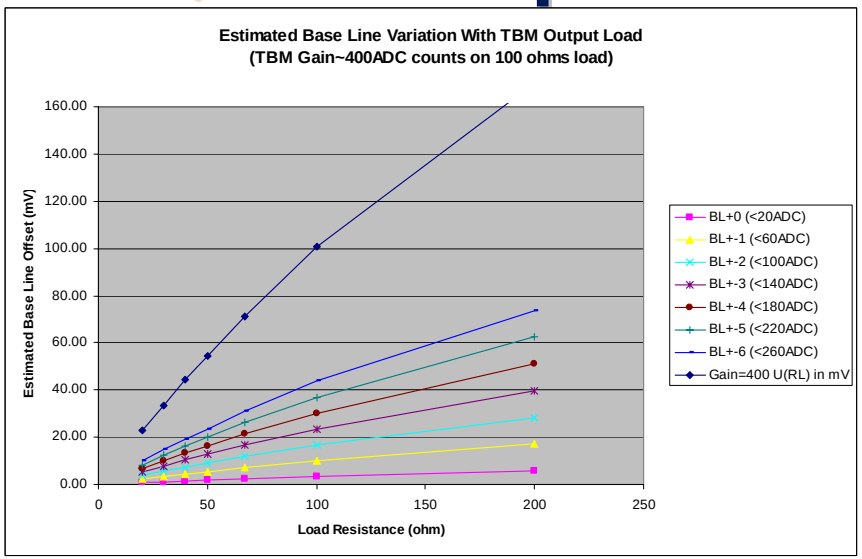
Base Line Classes Scenarios



Base Line Classes Scenarios



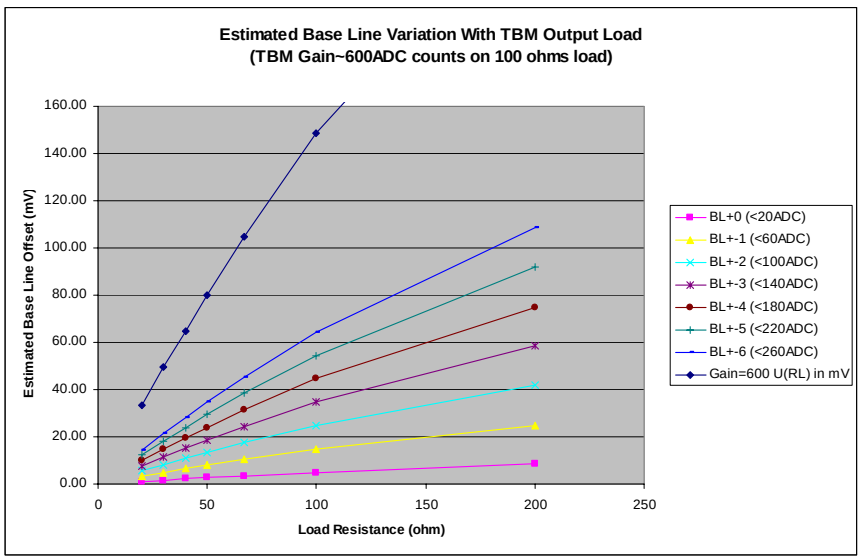
Estimated Base Line Dependence On Load Resistor

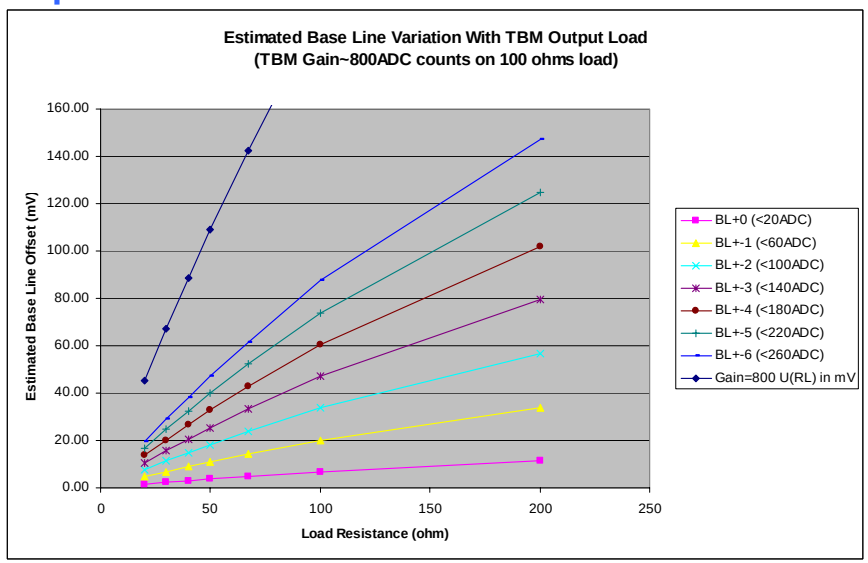


It is difficult to estimate the Base Line Offset for other loads because it is a random value, different for A and B sections and not correlated with Gain measurements.

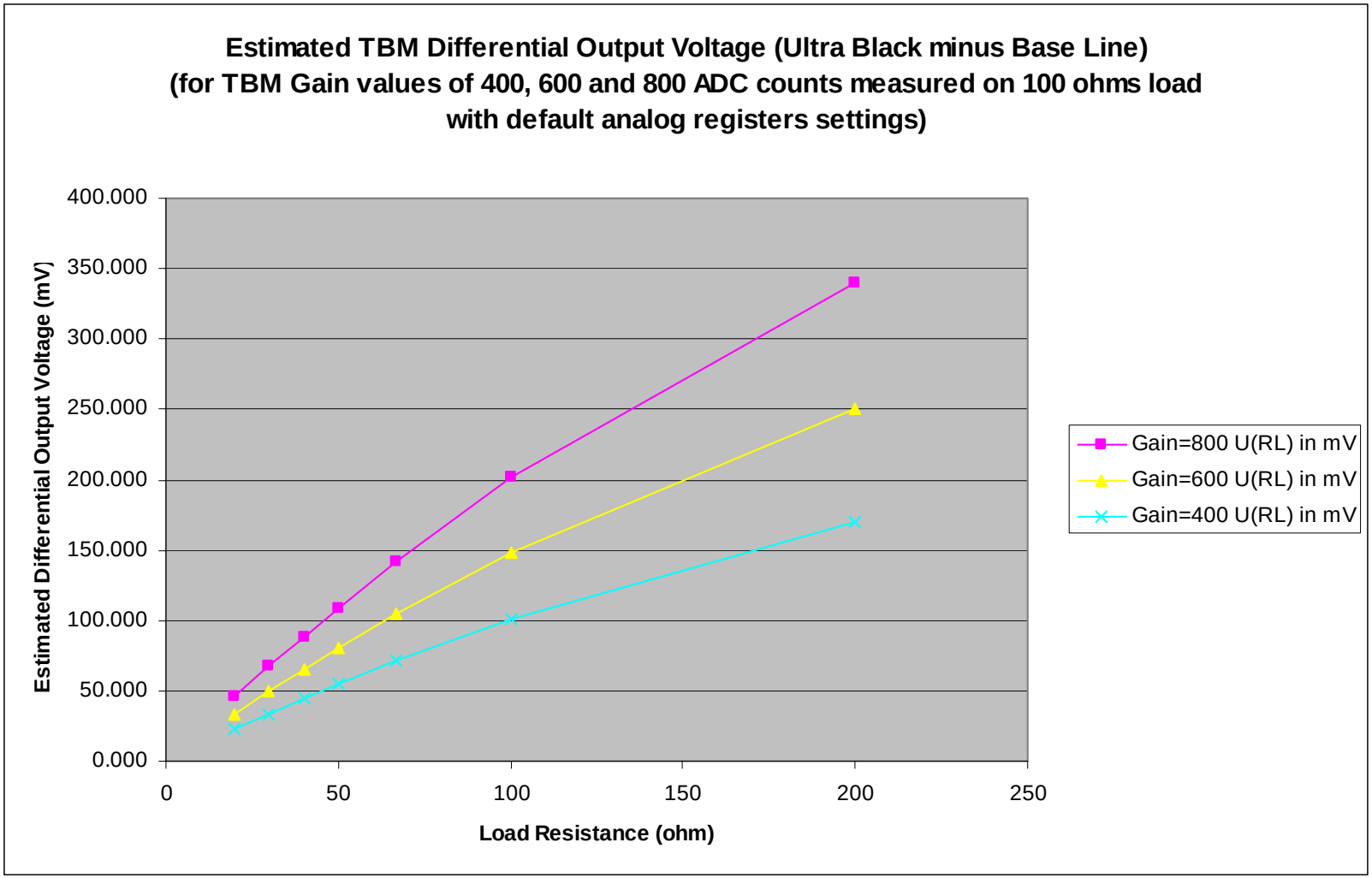
Just for a first order estimate, we'll assume that it will scale down with RL the same way that the TBM Gain does. Using the same calculations presented elsewhere for Gain scaling, the Base Line Offset (mV) will scale as in these graphs.

The right way to impose a cut on accepted BL classes is to provide an absolute voltage offset based on module (system) requirements.





Estimated Gain Dependence On Load Resistor



Base Line Offset Normalized to Gain